Artificial-Line-Division Distributed ICs With 0.1-μm-Gate-Length GaAs MESFET and Three-Dimensional Transmission Lines

Shunji Kimura, *Member, IEEE*, Yuhki Imai, *Member, IEEE*, Satoshi Yamaguchi, *Member, IEEE*, Kiyomitsu Onodera, *Member, IEEE*, and Hiroyuki Kikuchi, *Member, IEEE*

***Abstract*—0.1-μm-gate-length GaAs MESFET distributed baseband integrated circuits (ICs) that utilize an artificial-line-division technique and three-dimensional transmission lines are described. The technique reduces return loss of the distributed circuits at high frequencies, and four-layer transmission-line structure reduces parasitic impedance caused by the IC pattern shape and is suitable for the flip-chip bonding module format. A gate-line-division distributed baseband amplifier IC achieved input return loss of less than −13 dB and gain of 11.7 dB in the 0–56-GHz band. A source-line-division distributed level-shift IC achieved output return loss of less than −9.6 dB at high frequencies and insertion loss of 2.7 dB in the 0–79-GHz band. Both results better the performance of all reported GaAs MESFET distributed ICs.**

***Index Terms*—Distributed amplifier, GaAs MESFET, level-shift circuit, optical transmission, three-dimensional transmission line.**

I. Introduction

FUTURE multimedia communications will require higher speed transmission systems. 10-Gbit/s-class integrated circuits (ICs) have already been developed [1] and focus is now being placed on constructing 40-Gbit/s-class devices. The baseband amplifier is one of the most important components of such systems. The amplifier should have wide-band characteristics extending from 8 kHz [2] to several tens of gigahertz.

Distributed amplifiers are currently being designed as baseband amplifiers because of their potential wide-band characteristics [2], [4]. These amplifiers, however, do not have a good input return loss (S_{11}) at high frequencies because the cutoff frequency of the gate line is lower than that of the drain line.

Moreover, distributed amplifiers inherently have poor gain. A cascaded distributed amplifier can produce higher gain, but a large coupling capacitor cannot be monolithically integrated on the same chip, and chip capacitors do not have good high-frequency performance. As one solution, distributed level-shift circuits (DLSCs) [5] are being used to couple the amplifiers because these circuits have better wide-band characteristics than distributed amplifiers and because the direct-coupled configuration allows the lower limit frequency of the cascaded amplifier to be 0 Hz (dc). However, the DLSC does not have good output return loss (S_{22}) at high frequencies. This is because the output impedance of the circuit increases at high frequencies.

Aside from this, the parasitic impedance caused by the IC pattern shapes degrade the IC performance, and the bonding wires and conventional package structures also cause poor module performance.

This paper first proposes a new design technique called "artificial-line division," which reduces the high-frequency return loss of the circuits. Next, our 0.1-μm-gate-length GaAs MESFET and a three-dimensional IC structure suitable for the flip-chip bonding module format are described. Finally, experimental results for ICs that incorporate these techniques are presented.

Manuscript received May 1, 1998; revised September 13, 2001.

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Publisher Item Identifier S 0018-9480(02)05223-7.

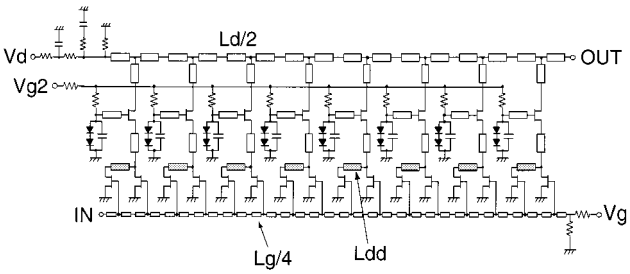


Fig. 1. Circuit schematic of the gate-line-division DBA.

II. Circuit Design

We propose artificial-line-division techniques to reduce the return loss of the distributed baseband amplifier (DBA) and the DLSC. The theories of the improvements are described as follows.

A. Gate-Line-Division DBA

The circuit schematic of the "gate-line-division" DBA is shown in Fig. 1. The key features of this design are divided common-source transistors of the cascode pairs and multiple transmission lines $(L_{\rm dd})$ between the drain terminals of the divided transistors.

Conventionally designed DBAs do not have good input return loss (S_{11}) at high frequencies because the cutoff frequency of the gate line is lower than that of the drain line. This is due to the fact that the gate-to-source capacitance $(C_{\rm gs})$ of the transistor is larger than the drain-to-source capacitance $(C_{\rm ds})$ under normal

bias conditions. The impedance- and velocity-matching conditions are

$$\sqrt{\frac{L_g}{C_{\rm gs}}} = \sqrt{\frac{L_d}{C_{\rm ds}}} \tag{1}$$

$$L_g C_{\rm gs} = L_d C_{\rm ds}. \tag{2}$$

Here, L_g and L_d are the per-section inductance of the gate and drain lines, respectively. If a DBA is designed with good velocity matching and wide-band characteristics, the optimized L_g value will be small and the image impedance of the gate line will become lower than the matching impedance. To improve the input matching characteristics, L_g should be optimized to a larger value. Consequently, the cutoff frequency of the gate line $(f_{\rm cg})$ will become lower than that of the drain line $(f_{\rm cd})$ and the velocity matching degrades.

When cascode transistor pairs are used, the output capacitance $(C_{\rm out})$ of each cascode pair becomes smaller than that of a single common-source transistor

$$C_{\rm out} \simeq \frac{C_{\rm ds}}{1 + \dfrac{C_{\rm ds}}{C_{\rm gs} + C_{\rm ds}}} < C_{\rm ds}. \tag{3}$$

The difference in capacitance between the input and output lines increases accordingly.

In the new design, the gatewidth of the common-source transistors is half that of the common-gate transistors. This doubles $f_{\rm cg}$ and improves S_{11} at high frequencies. The velocity difference at the drain terminals of the two divided transistors is compensated by an additional transmission line $L_{\rm dd}$. The condition, under which the velocity matching is improved, is formulated as follows.

If the constant-K-type-filter approximation is used, per-section phase constants of the gate and drain line are

$$\beta_g(f) = 2\sin^{-1}\frac{f}{f_{\rm cg}} \tag{4}$$

$$\beta_d(f) = 2\sin^{-1}\frac{f}{f_{\rm cd}} \tag{5}$$

$$\beta_{g'}(f) = 2N \cdot \sin^{-1}\frac{f}{N \cdot f_{\rm cg}}. \tag{6}$$

Here, $\beta_{g'}(f)$ is the per-section phase constant of the gate line divided among N common-source transistors. The velocity-matching-improvement condition is given as

$$int_0^{f_{\rm cg}}\beta_g(f)df - \int_0^{f_{\rm cg}}\beta_d(f)df > \int_0^{f_{\rm cg}}\beta_d(f)df - \int_0^{f_{\rm cg}}\beta_{g'}(f)df. \tag{7}$$

Each integrated term is

$$\int_0^{f_{\rm cg}}\beta_g(f)\,df = (\pi - 2)f_{\rm cg} \tag{8}$$

$$\int_0^{f_{\rm cg}}\beta_d(f)\,df = 2\left(f_{\rm cg}\sin^{-1}\frac{f_{\rm cg}}{f_{\rm cd}} + \sqrt{f_{\rm cd}^2 - f_{\rm cg}^2} - f_{\rm cd}\right) \tag{9}$$

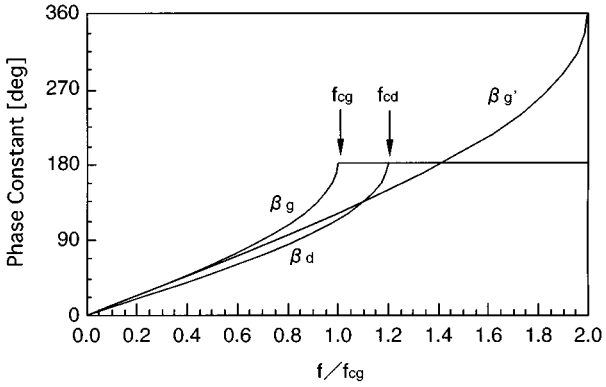


Fig. 2. Simulated per-section phase constants of the artificial lines.

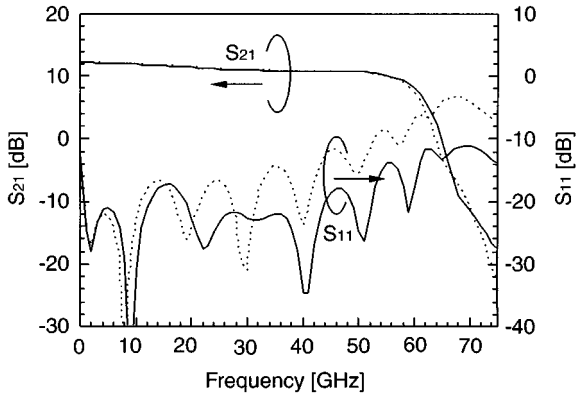


Fig. 3. Simulated S parameters of the DBAs. Solid line: gate-line-division amplifier. Dotted line: conventional amplifier.

$$\int_0^{f_{\rm cg}}\beta_{g'}(f)\,df = 2N\left(\sin^{-1}\frac{1}{N} + \sqrt{N^2 - 1} - N\right)f_{\rm cg}. \tag{10}$$

If we put (8)–(10) into (7) and assume that $N = 2$, (7) becomes

$$f_{\rm cd} \geq 1.037\, f_{\rm cg} \quad (C_{\rm gs} \geq 1.037\, C_{\rm out}). \tag{11}$$

Fig. 2 shows the simulated phase constants. The phase constant of the divided gate line is close to that of the drain line. Fig. 3 shows the effect of the gate-line division. The new circuit clearly has a lower S_{11} at high frequencies than the conventional circuit.

In addition to this technique, a loss-compensation circuit [3] is adopted to improve the high-frequency performance of the amplifier, and frequency-dependent drain termination [2] is adopted to achieve a flat gain starting from 0 Hz.

B. Source-Line-Division DLSC

Next, this "artificial-line-division" technique was applied to a DLSC [5]. In the conventional design (Fig. 4), the output return loss (S_{22}) at high frequencies is increased by the increase of the output impedance of the circuit. The origin of the increase is a quarter-wavelength resonance of the transmission lines. In the case of a DBA, the resonance frequency $(f_{\lambda/4})$ is negligibly higher than the cutoff frequency of the circuit. In the case of a DLSC, the $f_{\lambda/4}$ becomes relatively lower because the length of the transmission line is optimized to larger value to compensate the low output impedance of the source follower circuit.

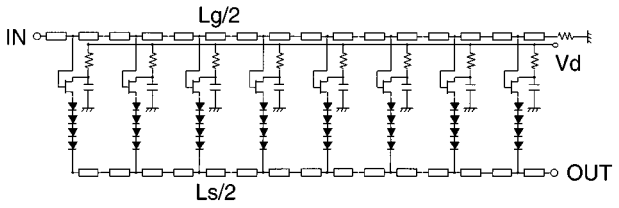


Fig. 4. Circuit schematic of the conventional DLSC.

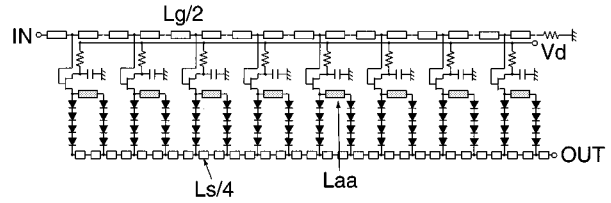


Fig. 5. Circuit schematic of the source-line-division DLSC.

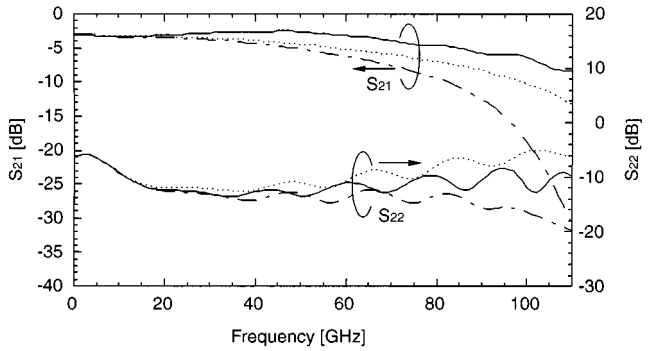


Fig. 6. Simulated S parameters of the DLSCs. Solid line: divided source line with $L_{\rm aa}$. Chain line: divided source line without $L_{\rm aa}$. Dotted line: conventional source line.

The schematic of the source-line-division DLSC is shown in Fig. 5. Key features of the design are the divided diodes and additional transmission lines $L_{\rm aa}$. In this case, the cutoff frequency of the source line does not double because the transistors are not divided. However, the length of the transmission lines on the source connection becomes half that of the conventional ones. Accordingly, $f_{\lambda/4}$ doubles and the output impedance decreases at high frequencies. This improves the impedance matching and reduces S_{22}, but the velocity matching between the two signal paths of the divided diodes is deteriorated. The line $L_{\rm aa}$ delays the signal on the right-hand side of the divided diode paths and compensates the degradation of the velocity matching.

Fig. 6 shows simulated S-parameters of the DLSCs. It is clear that the source-line division reduces S_{22}, but S_{21} is degraded by the degradation of the velocity matching. S_{21} is improved by the addition of $L_{\rm aa}$ compared to the conventional circuit. However, S_{22} is increased by this addition again, but they are still lower than those of the conventional circuit.

III. Fabrication

A gate-line-division DBA IC and the source-line-division distributed level-shift IC were fabricated using 0.1-μm gate-length GaAs MESFETs. The MESFETs have a planar structure that uses WSiN refractory metal as the Schottky gate. To prevent substrate leakage current, a new lightly doped drain structure was adopted with buried p-layers (BP-LDD). The 0.1-μm gate length is obtained by i-line photo lithography [6] and electron cyclotron resonance plasma-enhanced reactive ion etching (ECR plasma RIE) [7]. The MESFETs have an f_T of 100 GHz and $f_{\rm max}$ of 115 GHz. The transconductance (g_m) is 601 mS/mm. We used 50- and 25-μm-gatewidth transistors and operating voltages of $V_{\rm ds} = 1.5$ V and $V_{\rm gs} = 0.3$ V. In addition, 25-μm-gatewidth level-shift diodes were used with an operating voltage of 0.75 V.

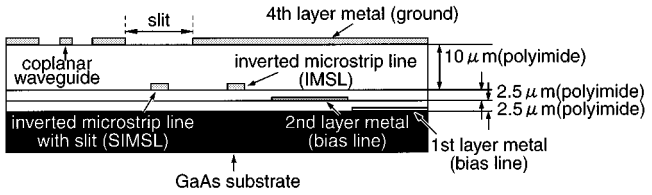


Fig. 7. Schematic structures of the three-dimensional transmission lines.

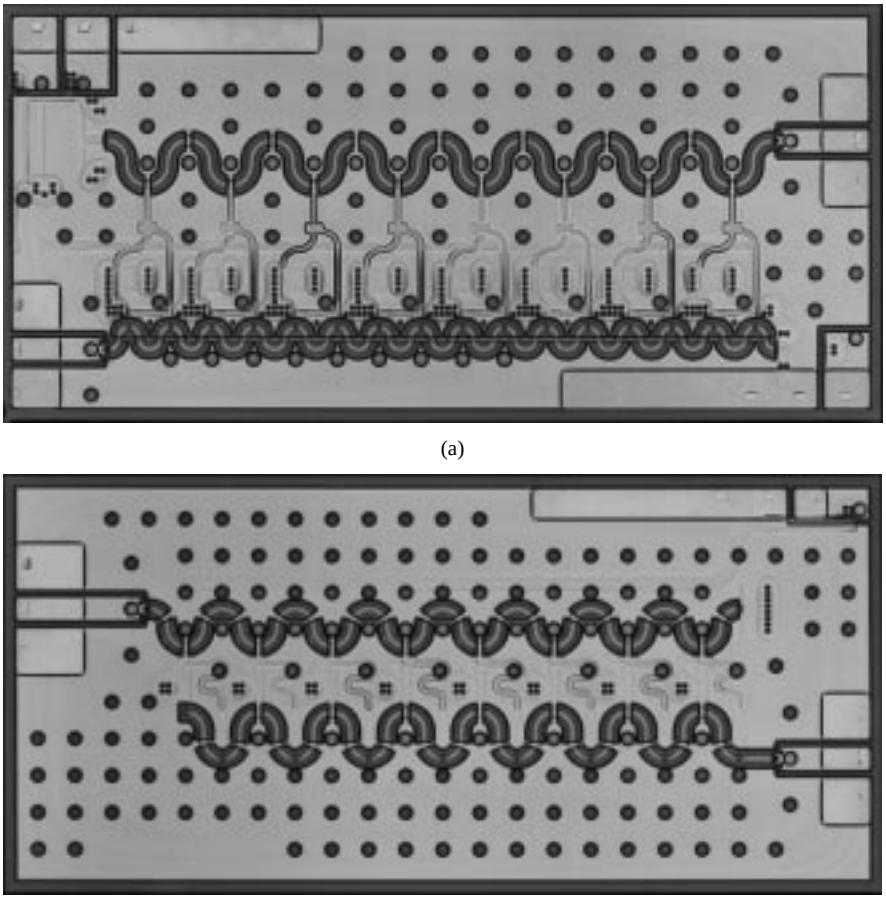
Also, a four-layer structure and novel inverted microstrip lines (IMSLs) [8] were used, as shown in Fig. 7, to suppress the parasitic impedance caused by the IC pattern shape and to suit the flip-chip bonding module format [9]. The fourth layer is grounded in this structure and the pads of the bumps are constructed above it. The ICs were designed to be mounted with flip-chip bonding. The transmission lines in the ICs are shielded by the fourth layer and do not divide the ground as conventional coplanar waveguides (CPWs) do. Thus, the parasitic impedance is caused only by the bumps and through holes. However, the attenuation of the IMSLs is higher than that of the conventional CPWs because the high-impedance IMSLs are narrow, while the conductor of the CPWs can be wide with wide gaps. Also, the effective dielectric constants of the IMSLs are smaller than those of the CPWs so IMSL length becomes larger than CPW length. To reduce the attenuation of the IMSL, we added a slit in the fourth-ground-layer metal. The IMSLs with the slit (SIMSLs) have lower attenuation and higher characteristic impedance. SIMSLs were used for only the main transmission lines of the artificial lines because the slits of the lines strengthen the parasitic impedance. Moreover, connective lines were added between the grounds divided by the slits. Microphotographs of the ICs are shown in Fig. 8. The size of both chips is 1.5 × 3 mm.

IV. Experimental Results

A. S Parameters

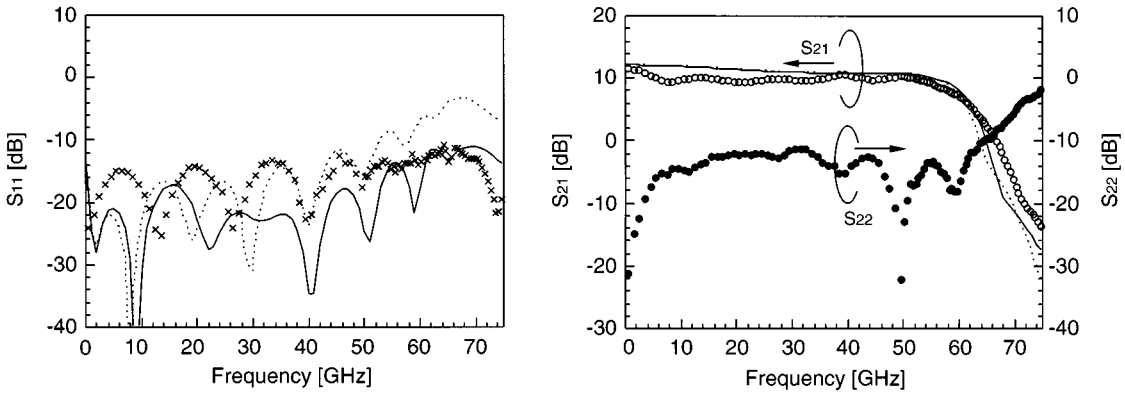
The frequency response was measured using on-wafer RF probes and a network analyzer. V- and W-band test sets and waveguide-input wafer probes were employed for over-50-GHz measurements.

Fig. 9 shows measured S-parameters of the gate-line-division DBA IC. The IC achieved the expected S_{11} of less than -13 dB at high frequencies [see Fig. 9(a)]. However, the S_{11} below 40 GHz could not match the simulated S_{11} well. We think that this is because the real transistor performance is slightly different from that of the simulated model. The IC has a maximum S_{21} of 11.7 dB, and S_{22} is less than -11.3 dB in the 0–56-GHz band [see Fig. 9(b)]. The gain bandwidth product (GBWP) achieved 215 GHz. This is the widest band and highest



(a) (b)

Fig. 8. Microphotographs of the artificial-line-division distributed ICs. (a) Gate-line-division DBA IC. (b) Source-line-division distributed level-shift IC.



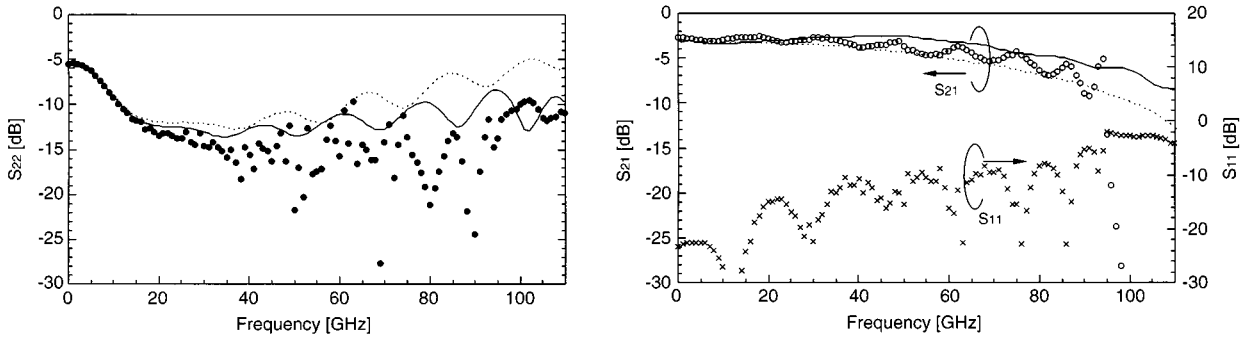
(a) (b)

Fig. 9. Measured S-parameters of the gate-line-division DBA IC. (a) S_{11}. Cross: measured S_{11}. Solid line: simulated S_{11} of the gate-line-division amplifier. Dotted line: simulated S_{11} of the conventional amplifier. (b) S_{21} and S_{22}. Open circle: measured S_{21}. Solid line: simulated S_{21} of the gate-line-division amplifier. Dotted line: simulated S_{21} of the conventional amplifier. Closed circle: measured S_{22}.

performance among all GaAs MESFET single-stage distributed amplifier ICs reported. The power dissipation is 1 W.

Fig. 10 shows measured S-parameters of the source-line-division distributed level-shift IC. As expected from the simulation, the IC achieved S_{22} of less than -9.6 dB at millimeter-wave frequencies [see Fig. 10(a)]. Moreover, S_{21} of -2.7 dB and S_{11} of less than -8.4 dB were achieved with the bandwidth of 79 GHz [see Fig. 10(b)]. This is also the widest band and highest performance of all reported level- shift ICs. We think that the origin of the difference between the simulated and measured S_{21} above 90 GHz is an unexpected resonance at 93 GHz caused by some parasitic effects on the gate line of the IC. The power dissipation is 0.55 W.

Aside from this, both ICs have a flat S_{21} from 0 Hz and are suitable for baseband applications without any off-chip components.



(a) (b)

Fig. 10. Measured S-parameters of the source-line-division distributed level-shift IC. (a) S_{22}. Closed circle: measured S_{22}. Solid line: simulated S_{22} of the source-line-division circuit. Dotted line: simulated S_{22} of the conventional circuit. (b) S_{21} and S_{11}. Open circle: measured S_{21}. Solid line: simulated S_{21} of the source-line-division circuit. Dotted line: simulated S_{21} of the conventional amplifier. Cross: measured S_{11}.

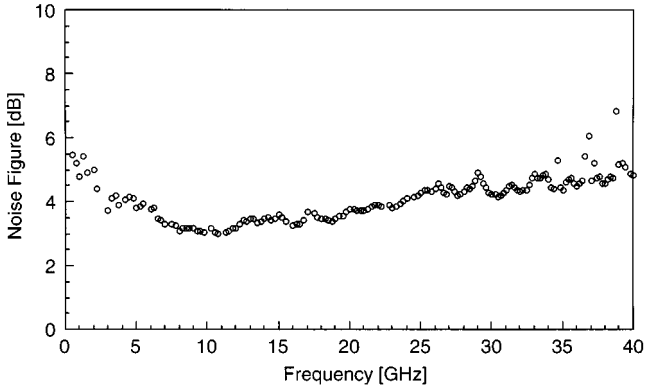


Fig. 11. Measured noise figure of the gate-line-division DBA IC.

B. Noise Figure

On-wafer measurements were performed using RF probes and a noise-figure meter. Only the amplifier IC was measured. The frequency range was 0.5–40 GHz. The measured noise figures are shown in Fig. 11. The average noise figure is 4.1 dB when the amplifier is biased for maximum gain.

V. Conclusion

In summary, we have described an advanced design technique for distributed circuits and showed measured performance results of ICs fabricated using the technique. A key feature is the artificial-line-division configuration, which reduces the high-frequency return loss of the distributed circuits. A gate-line-division DBA IC built around our 0.1-μm-gate-length GaAs MESFET achieves a S_{11} of less than -13 dB and a flat S_{21} of 11.7 dB in the 0–56-GHz band. The average noise figure is 4.1 dB in the 0.5–40-GHz band. A source-line-division distributed level-shift IC was also built using our MESFETs and achieved an S_{22} of less than -9.6 dB at high frequencies and a flat S_{21} of -2.7 dB in the 0–79-GHz band. These values better those of previously reported GaAs MESFET distributed ICs. Moreover, these are the first distributed ICs using a three-dimensional structure suitable for the flip-chip bonding module format.

We believe that our new technique will eliminate the electrical speed limitation of optical communication systems.

Acknowledgment

The authors thank Dr. S. Horiguchi, NTT Electronics Corporation, Tokyo, Japan, Prof. I. Kobayashi, University of Tokyo, Tokyo, Japan, Dr. K. Sato, NTT Network Innovation Laboratories, Nippon Telegraph and Telephone Corporation, Kanagawa, Japan, Prof. E. Sano, Hokkaido University, Hokkaido, Japan, and Dr. K. Yamasaki, NTT Electronics Corporation, Tokyo, Japan, for their encouragement and suggestions throughout this study.

References

[1] Y. Imai, E. Sano, and K. Asai, "Design and performance of wide-band GaAs MMIC's for high-speed optical communication systems," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 185–190, Feb. 1992.

[2] S. Kimura and Y. Imai, "0–40-GHz GaAs MESFET distributed baseband amplifier IC's for high-speed optical transmission," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 2076–2082, Nov. 1996.

[3] S. Kimura, Y. Imai, Y. Umeda, and T. Enoki, "Loss-compensated distributed baseband amplifier IC's for optical transmission systems," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 1688–1693, Oct. 1996.

[4] J. Pusl, B. Agarwal, R. Pullela, L. D. Nguyen, M. V. Le, M. J. W. Rodwell, L. Larsen, J. F. Jensen, R. Y. Yu, and M. G. Case, "Capacitive-division traveling-wave amplifier with 340 GHz gain-bandwidth product," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, May 1995, pp. 1661–1664.

[5] S. Kimura, Y. Imai, and Y. Miyamoto, "Direct-coupled distributed baseband amplifier IC's for 40-Gbit/s optical communication," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1374–1379, Oct. 1996.

[6] K. Nishimura, K. Onodera, S. Aoyama, M. Tokumitsu, and K. Yamasaki, "High performance 0.1-μm-self-aligned-gate MESFET technology," in *Proc. 26th Eur. Solid State Dev. Res. Conf.*, Sept. 1996, pp. 865–868.

[7] Y. Yamane, M. Tokumitsu, K. Nishimura, and K. Inoue, "0.1-μm GaAs MESFET's fabricated using ion-implantation and photo-lithography," in *IEEE GaAs IC Symp. Dig.*, Oct. 1993, pp. 117–120.

[8] S. Yamaguchi, Y. Imai, T. Shibata, T. Otsuji, M. Hirano, and E. Sano, "An inverted microstrip line IC structure for ultra high-speed applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, May 1995, pp. 1643–1646.

[9] S. Yamaguchi, Y. Imai, S. Kimura, and H. Tsunetsugu, "New module structure using flip-chip technology for high-speed optical communication IC's," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, June 1996, pp. 243–246.

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